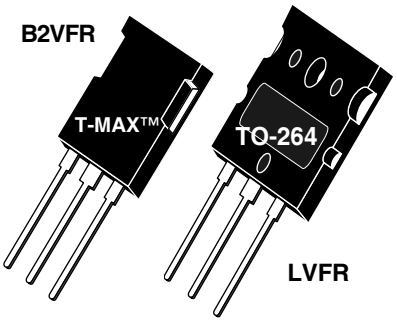
APT10M09B2VFR
APT10M09LVFR

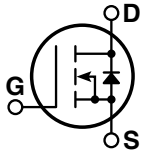
100V 100A 0.009Ω

POWER MOS V® FREDFET



Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.

- **T-MAX™ or TO-264 Package**
- **Avalanche Energy Rated**
- **Faster Switching**
- **FAST RECOVERY BODY DIODE**
- **Lower Leakage**



MAXIMUM RATINGS All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT10M09B2VFR_LVFR	UNIT
V_{DSS}	Drain-Source Voltage	100	Volts
I_D	Continuous Drain Current ⑥ @ T_C = 25°C	100	Amps
I_{DM}	Pulsed Drain Current ①	400	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ T_C = 25°C	625	Watts
	Linear Derating Factor	5.00	W/°C
T_J,T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ① (Repetitive and Non-Repetitive)	100	Amps
E_{AR}	Repetitive Avalanche Energy ①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ④	3000	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage (V_{GS} = 0V, I_D = 250μA)	100			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ② (V_{GS} = 10V, I_D = 50A)			0.009	Ohms
I_{DSS}	Zero Gate Voltage Drain Current (V_{DS} = 100V, V_{GS} = 0V)			100	μA
	Zero Gate Voltage Drain Current (V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C)			500	
I_{GSS}	Gate-Source Leakage Current (V_{GS} = ±30V, V_{DS} = 0V)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 2.5mA)	2		4	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1 MHz		9875		pF
C_{oss}	Output Capacitance			3940		
C_{rss}	Reverse Transfer Capacitance			1470		
Q_g	Total Gate Charge ③	V_{GS} = 10V V_{DD} = 50V I_D = 100A @ 25°C		350		nC
Q_{gs}	Gate-Source Charge			60		
Q_{gd}	Gate-Drain ("Miller") Charge			180		
$t_{d(on)}$	Turn-on Delay Time	V_{GS} = 15V V_{DD} = 50V I_D = 100A @ 25°C R_G = 0.6Ω		18		ns
t_r	Rise Time			36		
$t_{d(off)}$	Turn-off Delay Time			50		
t_f	Fall Time			9		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions		MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)				100	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)				400	
V_{SD}	Diode Forward Voltage ② (V_{GS} = 0V, I_S = -100A)				1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤				8	V/ns
t_{rr}	Reverse Recovery Time (I_S = -100A, di/dt = 100A/µs)	T_j = 25°C			190	ns
		T_j = 125°C			370	
Q_{rr}	Reverse Recovery Charge (I_S = -100A, di/dt = 100A/µs)	T_j = 25°C		0.4		µC
		T_j = 125°C		1.7		
I_{RRM}	Peak Recovery Current (I_S = -100A, di/dt = 100A/µs)	T_j = 25°C		9		Amps
		T_j = 125°C		15		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.20	°C/W
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 µs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T_j = +25°C, L = 0.60mH, R_G = 25Ω, Peak I_L = 100A

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \le -I_D 100A$ $di/dt \le 200A/\mu s$ $V_R \le 100V$ $T_J \le 150°C$

⑥ The maximum current is limited by lead temperature.

APT Reserves the right to change, without notice, the specifications and information contained herein.

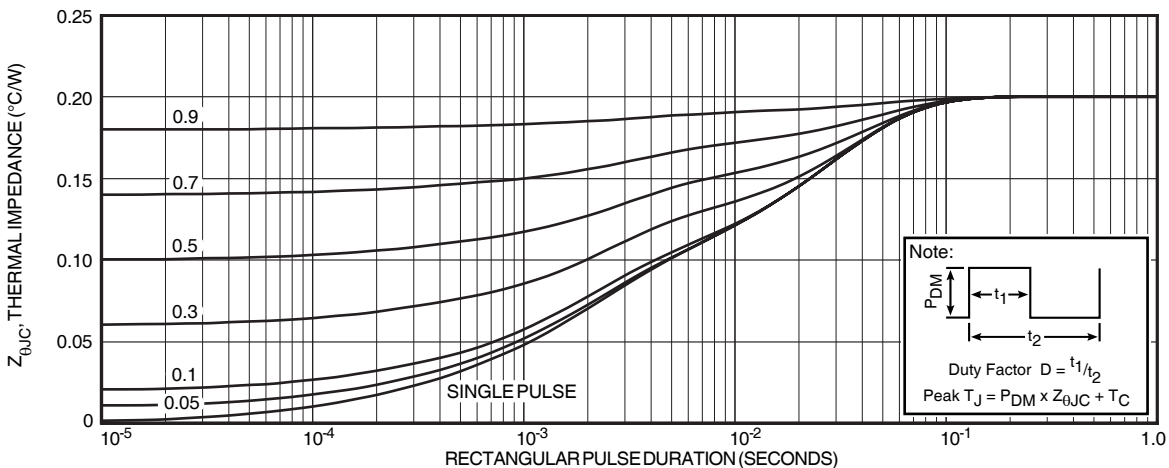


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

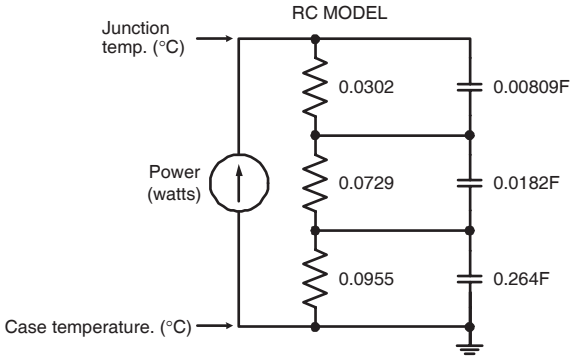


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

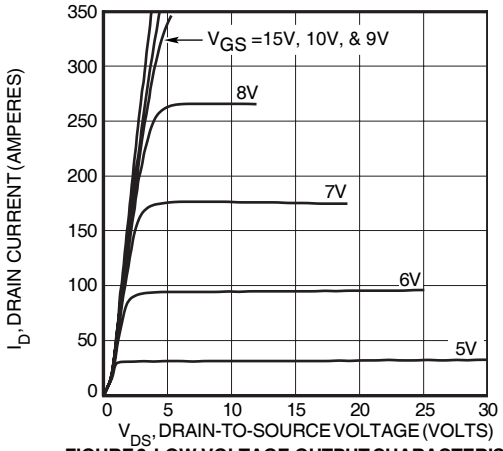


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

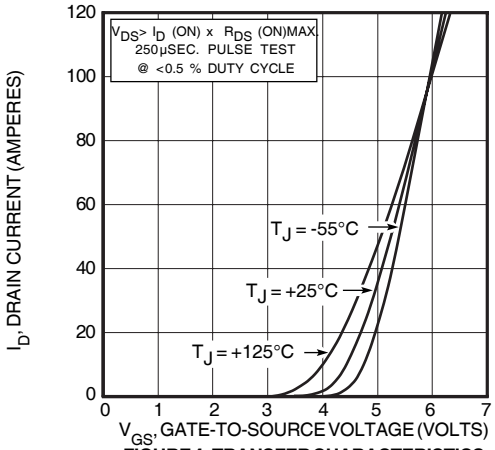


FIGURE 4, TRANSFER CHARACTERISTICS

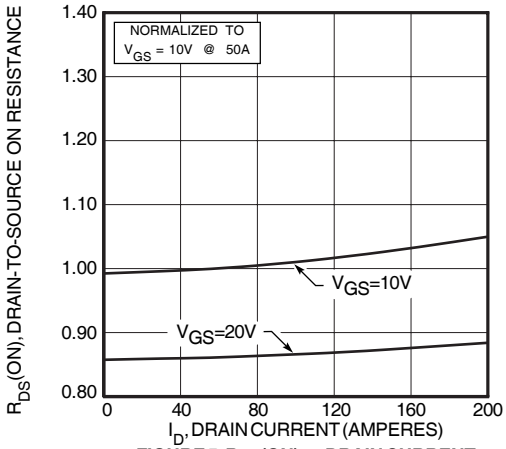


FIGURE 5, R_{DS}(ON) vs DRAIN CURRENT

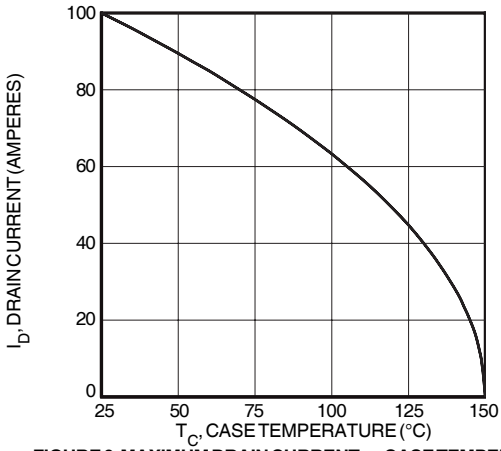


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

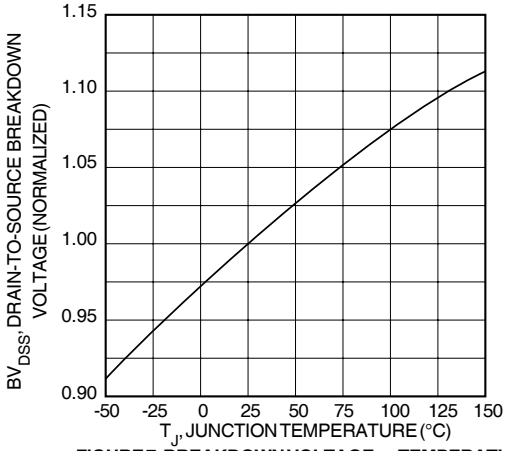


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

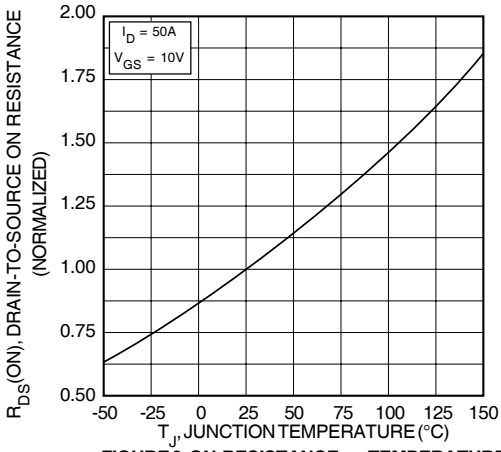


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

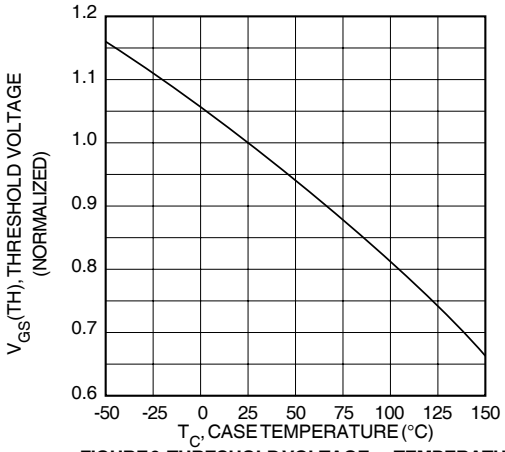


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

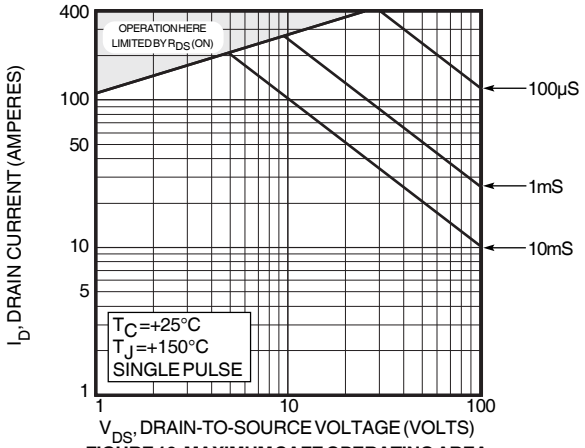


FIGURE 10, MAXIMUM SAFE OPERATING AREA

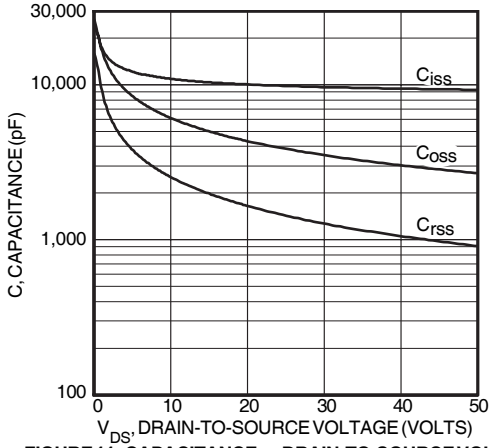


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

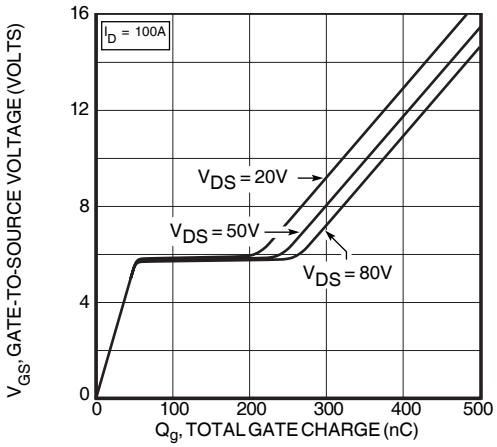


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

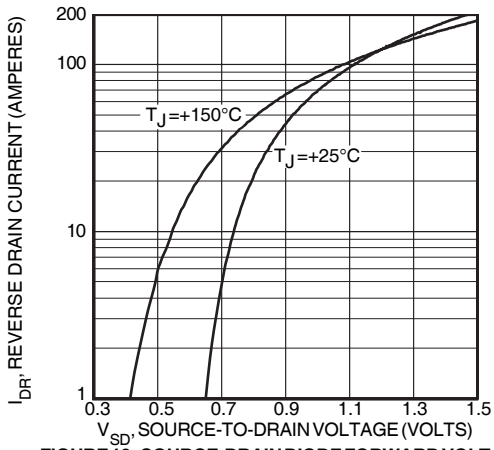
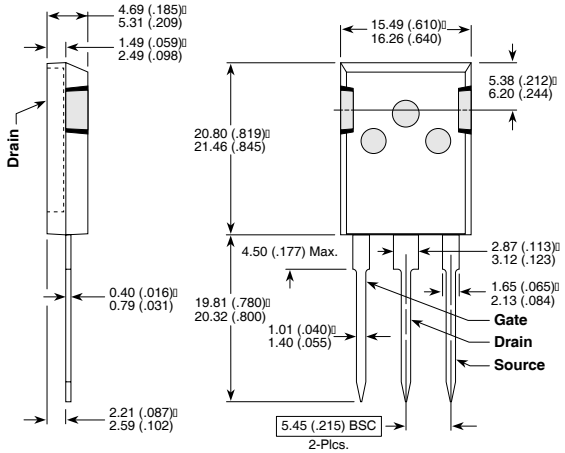


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

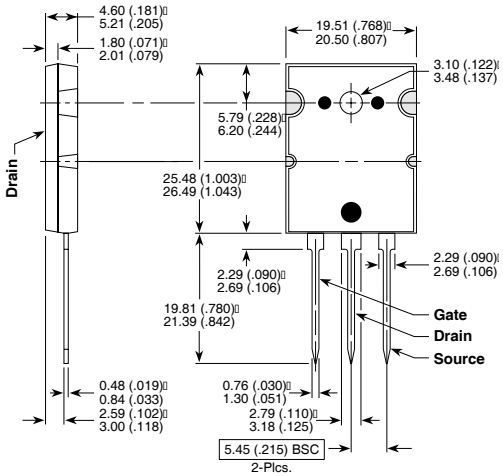
T-MAX™ (B2) Package Outline (B2VFR)



These dimensions are equal to the TO-247 without the mounting hole.

Dimensions in Millimeters and (Inches)

TO-264 (L) Package Outline (LVFR)



Dimensions in Millimeters and (Inches)

APT's products are covered by one or more of U.S.patents 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336 6,503,786 5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058 and foreign patents. US and Foreign patents pending. All Rights Reserved.